WIP: Towards a Georgia Tech Semiconductor Experience for Underclassmen

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***Abstract*—This work in progress innovative practice paper describes the plans of a semiconductor experience tailored to underclassmen engineering students. The Georgia Tech Semiconductor Experience (GTSE) is an upcoming program that is to provide a first-year experience that inspires pursuit of a career in semiconductor technology. Initially acting as a project that may be chosen and completed during a freshmen electrical and computer engineering course, GTSE will provide an opportunity for underclassmen to acquire a glimpse into the fabrication, modeling, and visualization of semiconductor-related devices. Fabrication consists of processes needed to fabricate a silicon solar cell. The fabrication process has been developed to maximize student safety, maximize student throughput each semester, and minimize the processing complexity. Processes requiring experience will be done under the guidance of a teacher assistant or instructor. After fabrication, the solar cells will be tested to determine their I/V characteristics and efficiency. The data can then be used to help students understand the complexity that a non-ideal world can introduce in a relatively simple device. The outcome of the semiconductor fabrication process is simulated using Silvaco Athena, and modeling of the solar cell device's electrical and physical properties is accomplished using Synopsys TCAD. Visualization of semiconductor device operation and atomic-level charge carrier operation is realized using custom software packages. To aid in the advancement of GTSE, underclassmen were asked to participate in guided research, modeling, or equipment setup and programming. Discussions about various aspects of silicon solar cell fabrication planning and modeling gave some qualitative insight into how well students will engage in the knowledge laid out for them. At the end of GTSE, students will have learned about various classical and quantum mechanics of the solar cell and understand the fabrication decisions. The main goal is to introduce basic skills and learning opportunities to spark interest in many semiconductor careers, especially since there is currently an industry demand for a semiconductor workforce in the United States.**

***Index Terms*—Semiconductor education, semiconductors, underclassmen education**

Intel Corporation

I. Introduction

As the semiconductor industry increases its footprint in the United States of America, there is an increased demand for a trained workforce in all related areas including integrated circuit design and semiconductor chip manufacturing. The need to increase the workforce in semiconductor technology has been well documented over the past several years [1] [2]. Workforce development is needed at all levels of education from 2-year degree programs through advanced graduate level education [3]. Much effort and focus has gone into semiconductor workforce development across the nation because of the CHIPS and Science Act, a U.S. federal statute enacted by the 117th United States Congress and signed into law by President Joe Biden on August 9, 2022 [4] [5] [6]. The act provides roughly $280 billion in new funding to boost domestic research and manufacturing of semiconductors in the United States CHIPS Act.

There are many efforts to address the need for a trained workforce in semiconductor technologies. Upon surveying the national landscape for semiconductor training at four-year degree institutions [7] [8] [9], it is unclear if there are programs for entry engineering level education. More extensive searching shows there are programs for graduate students [10] [11] and military members looking towards a semiconductor-related career [12].

There seems to be an important educational void to begin filling at the freshman and early sophomore level regarding semiconductor workforce development at 4-year academic institutions. What is missing? The Georgia Tech Semiconductor Experience (GTSE): An experience for incoming freshmen, sophomore, and transfer students to illicit interest in pursuing subsequent studies and future careers in semiconductors. It is important to include entry level students because they are just beginning to explore areas of education and want to see what there is to offer from various education and career

paths. The GTSE project is meant to provide an educationally flexible model to fill the national educational void. The GTSE is structured to minimize limitations on the number of seats available each semester. The program is planned to serve 100+ students per semester initially and grow the program from there.

GTSE Structure: The GTSE will be part of the new GT School of ECE Curriculum Partnership Initiative (CPI). By partnering with industry, the CPI ensures that students are equipped with relevant and up-to-date knowledge and practical experience. The CPI addresses the need for a quick ramp-up to industry by providing students opportunities for hands-on learning and exposure to real world problem-solving scenarios, ultimately enhancing students' readiness and employability upon graduation.

The GTSE project will provide an expandable platform through which GT underclassmen can obtain a self-tailored semiconductor experience based on their interest and degree major. Initially, the GTSE project will be implemented in the School of Electrical & Computer Engineering as a test bed. Subsequently, the GTSE will be expanded to include interested students from other GT schools across campus. Initial implementation of the GTSE in the GT School of ECE will be through the required course, ECE1100: Discovery Studio. All ECE students are required to take ECE1100 (Fall2023 enrollment: 260 students), and the course has a required self-guided student project as one of the course deliverables. The GTSE module(s) will serve to satisfy the self-guided student project component of the required ECE1100 course. As the GTSE expands to include other schools on campus, the GTSE will petition to become available to all GT students.

II. Planned Student Engagement

The GTSE will be composed of experiential learning modules (ELMs) for students. The ELMs allow for the student to gain expertise in areas of interest to them. Initially, the GTSE ECE ELMs will include the following ELMs:

1) Fabrication & Testing of a (100) Silicon Solar Cell
2) Silvaco Athena Modeling of the Solar Cell Fabrication Process
3) Silvaco TCAD Modeling of the Silicon Solar Cell Device
4) Atomic & Charge Carrier Visualization

As the GTSE grows from an ECE-centric program to an institute level program with a GTxxxx course number, it is anticipated to add ELMs from other schools to the GTSE for their students interested in participating in a semiconductor experience.

1) ELM#1: Fabrication & Testing of a Silicon Solar Cell : One of the core components of the GTSE is a hands-on student experience fabricating a semiconductor device. We have chosen the silicon solar cell as the exemplary semiconductor device for the ELMs for many reasons including the simplicity of the device, the simplicity of the fabrication process, the exemplary nature of the PN semiconductor junction, and the direct application of the photovoltaic technology to renewable energy. Figure 1 shows a cross-section of the basic commercial solar cell. This is the basic solar cell that will be fabricated and tested as part of ELM#1.

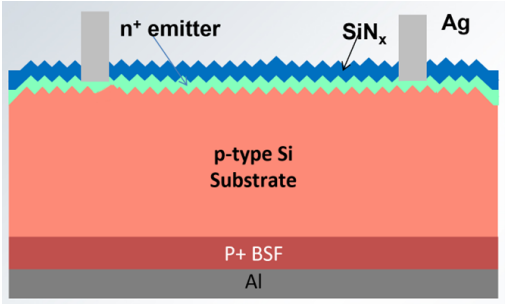

Fig. 1. The solar cell design to be fabricated and tested.

The fabrication process used to manufacture the solar cell includes a N-type impurity diffusion process, thin film deposition processes for silicon nitride and metallization layers, and photolithography and ink stenciling to fabricate the electrical contacts / metallization on the top and bottom of the silicon solar cell Figure 2. We plan to set up the solar cell fabrication facility in a standard non-cleanroom laboratory setting with hepa-filtered air for the processing steps that benefit the most (e.g., the photolithography process).

The fabrication process begins with a P+ wafer which has gone through the standard RCA semiconductor cleaning process and a field oxidation process. Photoresist is applied to protect the silicon dioxide on the backside of the wafer. Buffered Oxide Etchant (BOE) is used to remove silicon dioxide from the front-side of the silicon wafer. After the photoresist is removed, the wafer is uniformly doped on the front-side using a solid source boron nitride wafer, after which the residual borosilicate glass is removed using BOE. Subsequently, the drive-in process is used to establish an approximately 1.0 micrometers junction depth, and silicon dioxide layer is grown as part of the drive-in process. Once that doping process is complete, conductive aluminum paste is screen printed on the backside of the wafer to create one of the solar cell contacts. That paste is then annealed using a baking process on a hot plate. Once the back-side contact is established, the same screen-printing process is used on the front side of the wafer with silver paste and a specially designed contact mask which creates the contacts and busbars for the active surface of the solar cell. Once those are annealed in the same baking process, a spin-on glass AR coating is applied to the finished cell.

One of the guiding principles behind development of the GTSE is to minimize limitations on the number of students per semester enrolled in the GTSE. Towards this end, we will offer scheduled batch processing runs (2-3 per semester) for the impurity diffusion and the silicon nitride deposition processes. The equipment required for ELM#1 is 1. Diffusion furnace, 2. Oxidation furnace, 3. Mask Aligner, 4. Spin-cast station, 5. Ovens, 6. Screen printer, 7. Inspection Station, 8. Solar Cell Testing Station.

Expected Outcomes: Students should understand the signif-

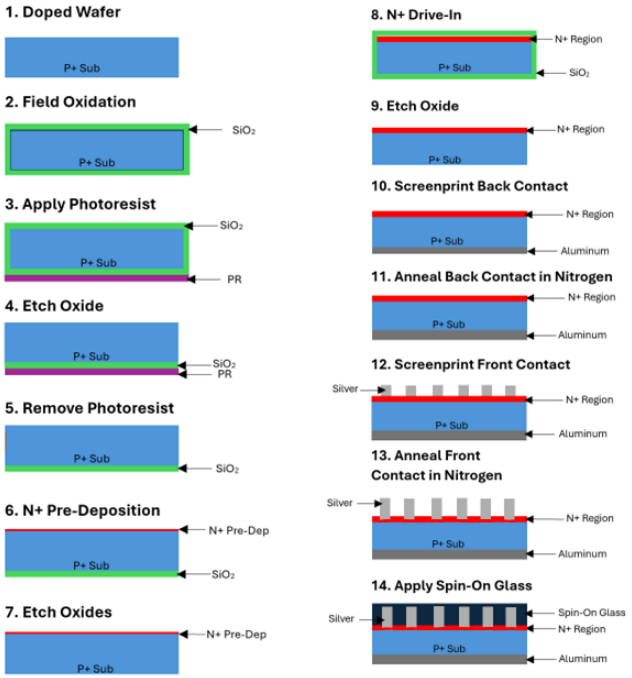

Fig. 2. Silicon solar cell fabrication process flow

icance of each step in the fabrication process. After learning about PN junctions and depletion regions through the modeling ELMS, students should be able to grasp the impact of the thermal processes. Students will perform and understand photolithography, spin-coating, and screen-printing procedures. Students should be able to perform solar cell testing. They should be able to interpret the results and understand how to determine the efficiency of the solar cell. With some background information, students should be able to understand what happens within the PN junction and why the solar cell produces varying power with changes in the light source power density.

2) ELM#2: Silvaco Athena Simulation of the Solar Cell Fabrication Process: One method for students to gain insight into manufacturing of semiconductor devices is through simulations of the manufacturing process. Process simulation software will be used to simulate the solar cell fabrication process to explore impurity concentrations, junction depths, silicon oxide thickness, and process variations. Towards the end of this effort, students will create two or more device structures suitable for device simulation and provide these results to the students engaged in the ELM 3 activity. Photovoltaic device simulations based on these device structures will in turn be provided to ELM 2 students by ELM 3 students, allowing the ELM 2 students to directly visualize changes in device operation affected by process variations. The Silvaco Athena software is currently available to students through Georgia Tech licensing agreements.

Expected Outcomes: Students are to have obtained a basic understanding of PN junctions. They should be able to program and simulate the doping thermal processes. They should know the significance of the junction depth and impurity profiles. Each student will be able to recognize how the model changes with varying thermal processes.

3) ELM#3: Synopsys TCAD Modeling of a Silicon Solar Cell: One method for students to gain insight into device operation is through device modeling and simulation. The Synopsys TCAD software will be used to model, simulate and visualize the operation of a photovoltaic device, with specific emphasis on how performance metrics including power generation and wall plug efficiency depend on design choices such as doping levels, layer thicknesses and top contact geometry. Towards the end of this effort, students will replace idealized device topology with the more realistic results of process simulation contributed by students engaged in the ELM 2 activity and be asked to compare simulation results and comment on the utility and accuracy of each choice of device structure model. The Synopsys TCAD software is currently available to students through Georgia Tech licensing agreements.

Expected Outcomes: Students will be able to run a simulated model of the solar cell to be fabricated. There will be discussion of the electrical properties of solar cells. Students will comprehend how the material properties can change electrical properties and be able to see these differences on graphs and models.

4) ELM#4: Atomic & Charge Carrier Visualization: We propose to use digital games and interactive visualizations to teach students the fundamentals of semiconductor physics and how devices such as PN junctions and solar cells work without using any mathematical formalism. Instead, the students will have the opportunity of observing and interacting with various physical phenomena such as atomic model of hydrogen atom, covalent bonding, quantized energy states and band structure, bandgap, electrons and holes, carrier generation and recombination, and carrier transport via drift and diffusion. Once they become familiar with these foundational concepts, they will be introduced to a PN junction, and they will see how a depletion layer is formed as a result of diffusion. Students will see how the device reaches equilibrium if no external voltage is applied and how this device can pass current in one direction and block current in the opposite direction. They finally have the opportunity to shine light on the PN junction to generate electron-hole pairs separated by the electric field inside the depletion region converting optical power to electric power, hence building a solar cell.

In Spring2023, working with an external evaluator, Naeemi's team conducted two formal evaluations regarding these educational tools. The first was a controlled study (N=29, where N is the number of students) comparing the visualizations to recorded lectures on topics in carrier statistics/transport for undergraduate students who had taken or were currently taking a microelectronics theory course at Georgia Tech. Each group completed a session involving a pre-test, intervention, post-test, followed by a focus group session. Quantitative analysis of students' pre-tests and post-tests found significant improvements ($p<0.01$, $d>0.9$, where p is the statistical p-value and d is Cohen's D) in student

engagement, self-efficacy, and motivation for the visualizations compared to recorded lectures, with similar learning gains. The second study was an end of semester survey (N=55) of an undergraduate microelectronics course which had employed the same visualizations differently in two different sections of the course. Students in the first section engaged with the visualizations in both the live lectures as well as homework, while those in the second only engaged with them for homework. The survey found significant improvements ($p<0.01$, $d>0.9$) in all three parameters for the first group and for self-efficacy in the second group.

A few guiding principles in the design and development of the visualizations include:

- Start from familiar then move to new concepts (e.g. classical to quantum mechanical concepts).
- Visualize the real and abstract concepts side by side (e.g. movement of electrons in real space vs. in energy-momentum diagram).
- Gradually add to the complexity by adding concepts one by one.
- Address common misconceptions.
- Have guiding text/questions at the side to allow independent study and experimentation and instructor-led exploration.
- For each concept, use innovative approaches to best help students learn the concepts.
- Make it interesting and educational for students at different levels of proficiency by incorporating advanced topics that can be ignored by less advanced students.

Expected Outcomes: Students should have a basic understanding of semiconductor material quantum mechanical characteristics, and they will have a mental image of carrier position in energy band diagrams and current transport mechanisms. Students will be able to visualize PN junction currents and band diagrams with applied voltage or as a solar cell.

III. Experience Working with First-Year Students

During Fall2023, students from Georgia Tech's ECE 1100 class began providing information that pertained to the planned GTSE. They were broken up into five groups: Synopsys TCAD modeling, Silvaco Athena modeling, fabrication, mask design, and solar cell testing. These students were given guidance about performing their own research and asked to find pertinent information. There were 17 students, and most of them were able to contribute to information gathering and/or modeling.

Before the students could research on their own, they were given basic information about PN junctions and desired solar cell characteristics. After having a couple of weeks of research and background information, many students in the fabrication and Athena modeling groups had an idea of how the cell should be designed or modeled. By the end of the semester, the fabrication team developed a partial process, and the Athena modeling group simulated the thermal processes to give impurity profiles that would later be adjusted.

Since Silvaco Athena can be a relatively simple program, the team was able to simulate the creation of a PN junction, but Synopsys TCAD modeling progress was limited. Synopsys TCAD was found to be more advanced and required more time to become acquainted. Given the limited experience with such a tool, the ECE 1100 students were only expected to be able to access the program and run an example simulation, and this was done successfully. A simpler option, Silvaco TCAD modeling software, will be explored for future TCAD modeling.

The mask design team explored the design of the solar cell topside and backside contacts. The students learned about the basic principles of designing the top electrode and designed a mask reflecting what they learned. The testing team was tasked with determining solar cell station sources but was unable to source a system at the time.

The Spring2024 ECE 1100 group consisted of 7 students. Each student worked with the senior design team and performed various tasks to progress GTSE's foundation.

Overall, the ECE 1100 students were engaged in assigned tasks by asking questions and bringing forth information. Though they lacked a lot of the background information required to fully understand the reasoning behind the processes and simulations, most were able to quickly learn through self-study and limited guidance. In addition to the students' academic exploration, many tasks were performed well and in a timely manner.

IV. Future Progress Planning

Spring2024 showed significant progress in laboratory setup and modeling program exploration, but there is still much work to be done. The following sections give some general information about what is needed to complete Phase 1 of the GTSE.

A. Fabrication Laboratory Preparations

Equipment in the laboratory has undergone maintenance and upgrades to ensure proper functionality. More trial runs of the furnace equipment will be required to determine if program debugging is required and if processes can be carried out consistently. While there may still be some light maintenance to occur, there is general organization and tidying up to take place.

As the lab's mechanical and program aspects are adjusted, instructions and safety protocols are to be written. Instructions will be made for every program and piece of equipment students are expected to use. Safety protocols will be written and include institute plans that ensure compliance with Georgia Tech's policies regarding laboratory usage and emergency planning.

B. Course Self-Learning Modules

Each of the ELMs has underlying technical content that can be delivered to students via self-learning modules. A series of course self-learning modules to support the GTSE are to be produced. The self-learning modules would include reading

materials and presentations/lectures for students. For example, in the case of ELM#1: Fabrication & Testing of a silicon solar cell, the fabrication processes include thermal diffusion of dopants in silicon, oxidation of silicon, photolithography, screen printing, spin-casting, and testing. An introduction to and presentation of the underlying theoretical materials for the fabrication processes can be supported by recorded lectures and presentation materials. Similarly, self-learning modules for the modeling and visualization ELMs must be generated.

C. Expansion of the GTSE

As the GTSE matures, he GTSE is planned to expand and include other schools at Georgia Tech with an interest in various aspects of renewable energy, semiconductor materials and processes, semiconductor packaging, etc. Extension into other schools will be accompanied by the development of additional ELMS such as materials-related modules, packaging-related modules, or alternative solar cell processing modules such as perovskite cell production. Schools of interest include Materials Science and Engineering, Mechanical Engineering, and Chemical Engineering.

D. Student Evaluation

Students taking part in the GTSE will need to be evaluated to determine how well they understand the material. This area still requires more planning for all ELMs. Also, noting how well students do in later semiconductor-related courses would provide great insight into the GTSE effectiveness.

E. Conclusion

This paper is meant to inform of GT's effort to encourage student interest in the semiconductor career field. GTSE is a work-in-progress with much promise to provide valuable information and physical participation in the world of semiconductors. Interaction and exploration are hoped to spark passion for semiconductor-related fields in students still exploring educational possibilities. Perhaps, the GTSE will prove to inspiration for similar programs to be produced at other universities.

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